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56. Prior art publications taken into consideration for the determination of patentability:

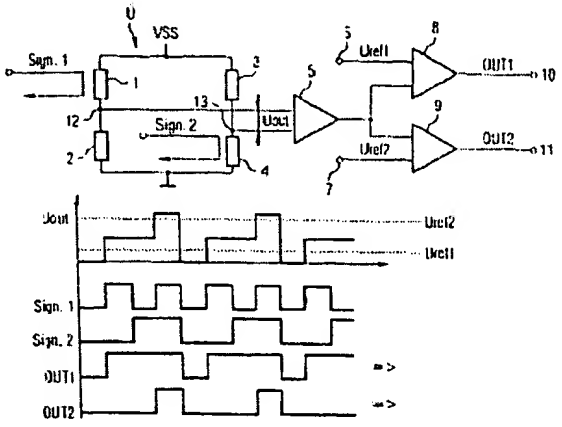
DE 197 18 420 A1
DE 20 02 693
US 54 42 303

54. Integrated circuit for generating a drive signal for an Isolated Gate Bipolar Transistor (IGBT)

57. The invention relates to a method and a device for the logical combination of signals. The signals to be combined with one another are fed on separate signal lines to a transmitter having a magneto-sensitive coupling element, where the signals are transmitted in electrical isolation and are detected by a magneto-sensitive detector of the respective coupling element. Connected with the magneto-sensitive detectors is an evaluation unit, at the output or outputs of which the desired resulting signals are made available in electrically isolated form.

OR

AND



Description

This invention relates to a method and a device for the logical combination of signals.

Semiconductor elements that are manufactured in the form of integrated circuits are generally used to realize logical combinations of signals. The book entitled "Halbleiter-Schaltungstechnik" *[Semiconductor Circuit Technology]* by U. Tietze and Ch. Schenk, 9th Edition, published by Springer Verlag 1990, describes a number of such semiconductor components. For example, AND operations, OR operations, multiplexing, demultiplexing and other logic operations can be realized using semiconductor components.

DE-197 18 420 A1 describes integrated data transmission circuitry of the prior art with electrical isolation between the input and output circuit. This circuitry of the prior art has an integrated, magneto-sensitive coupling element, by means of which the binary input signals fed to the input circuit are transmitted to the output circuit and are made available at its output in binary form. By means of the magneto-sensitive coupling element, a magnetic field which is generated in the vicinity of a conductor loop and varies as a function of the input signal is detected and is forwarded in the form of the above mentioned binary signals. The magneto-sensitive coupling can be realized in the form of a Hall-effect generator, an anisotropic magnetic resistance (AMR) component, a giant magneto-sensitive (GMR) component or a tunneling magneto-sensitive (TMR) component.

On the basis of this prior art, the object of the invention is to provide a new method and a new device for the logic combination of signals.

The invention teaches that this object can be accomplished by a method having the features disclosed in Claim 1 and by a device having the features disclosed in Claim 4. Advantageous realizations and developments of the invention are disclosed in the subclaims.

The advantages of the invention include the fact that it can be realized easily and economically in applications in which an electrical isolation is achieved with the use of magneto-sensitive components that are already present. Applications of this type can

be found, in particular, in sensor technology in which signals acquired by means of a sensor element must be transmitted in an isolated manner to achieve a galvanic separation. Applications of this type also include those in which MRAMs are used for storage of the signal in a digital circuit. These memories are magnetic memories which retain their memory status so that no refresh process is necessary.

Additional advantageous characteristics of the invention are indicated in the following explanation of the exemplary embodiments illustrated in the accompanying figures, in which:

Figure 1 shows a first exemplary embodiment of the invention,

Figure 2 shows a second exemplary embodiment of the invention,

Figure 3 shows a third exemplary embodiment of the embodiment,

and

Figure 4 shows a fourth exemplary embodiment of the invention.

Figure 1 shows a first exemplary embodiment of the invention. In a first exemplary embodiment, the two input signals Sign. 1 and Sign. 2 fed to the illustrated circuit on separate signal lines are to be combined with each other for the performance of an AND logic operation and/or an OR logic operation.

For this purpose, the above mentioned input signals are fed to a transmitter Ü where they are each delivered to a conductor loop in the vicinity of respective magneto-sensitive detectors 1 or 4. These detectors are a component of a parallel circuit with two paths located between a power supply connection V_{SS} and the ground. In the first path there are magneto-sensitive detectors 1 and 2 in the form of a series circuit. The second path contains magneto-sensitive detectors 3 and 4, which also form a series circuit. From the connection point 12 between the magneto-sensitive detectors 1 and 2, a signal connection leads to an input of a first differential amplifier 5. Its other input is connected with the connection point 13 between the two magneto-sensitive detectors 3 and 4.

Connected to the output of the first differential amplifier 5 are two additional differential amplifiers 8 and 9 which are arranged parallel to each other. A reference voltage U_{ref1} derived from a reference voltage input 6 is fed to the additional input of the

differential amplifier 8. The other input of the differential amplifier 9 is connected with an input 7 to which a reference voltage U_{ref2} is applied.

At the output 10 of the differential amplifier 8, a resulting signal OUT1 can be picked off, which corresponds to an OR logic operation involving the two input signals Sign. 1 and Sign. 2. This resulting signal OUT1 is available electrically isolated from the above mentioned input signals.

At the output 11 of the differential amplifier 9, a resulting signal OUT2 can be picked up, which corresponds to an AND logic operation involving the two input signals Sign. 1 and Sign. 2. This resulting signal OUT2 is also available electrically isolated from the above mentioned input signals.

Underneath the block diagrams shown in Figure 1, signal waveforms of the signals that are presented in the block diagram are presented. The signals Sign. 1 and Sign. 2 to be combined with each other are digital signals. U_{out} designates the voltage between the circuit points 12 and 13 which corresponds to the voltage between the two inputs of the first differential amplifier 5. U_{ref1} and U_{ref2} are the reference voltages which are applied to the inputs 6 and 7 of the illustrated circuit. Finally, OUT1 and OUT2 are the resulting signals that can be picked off from the outputs 10 and 11, and which correspond to the desired OR and AND logic operation on the input signals Sign. 1 and Sign. 2. These resulting signals are available electrically isolated from the input signals.

Figure 2 shows a second exemplary embodiment of the invention. In this exemplary embodiment, the two input signals Sign. 1 and Sign. 2 fed to the illustrated circuit on separate signal lines are combined with each other so that a selection of parts of the signal Sign. 1 is made by means of the signal Sign. 2.

For this purpose, the above mentioned input signals are fed to a transmitter Ü where, with the use of a conductor loop, they are conducted to the vicinity of respective magneto-sensitive detectors 1 and 3. These detectors are components of a parallel circuit with two paths provided between a power source connection V_{SS} and ground. In the first path are magneto-sensitive detectors 1 and 2 in the form of a series circuit. The second path contains magneto-sensitive detectors 3 and 4 which also form a series circuit. From the connecting point 12 between the magneto-sensitive detectors 1 and 2 a signal connection leads to an input of a first differential amplifier 5. Its other input is

connected with the connecting point 13 between the two magneto-sensitive detectors 3 and 4.

Connected to the output of the first differential amplifier 5 is an additional differential amplifier 14. A reference voltage U_{ref} derived from a reference voltage input 15 is fed to the additional input of this differential amplifier 14.

At the output 16 of the differential amplifier 14, a resulting signal OUT can be picked off which corresponds to segments of the signal Sign. 1 selected by means of the signal Sign. 2. This resulting signal OUT is available electrically isolated from the above mentioned input signals.

Below the block diagram in Figure 2, signal waveforms are shown for the signals that are illustrated in the block diagram. The signals Sign. 1 and Sign. 2 to be combined with each other are each rectangular pulse signals. U_{out} is the voltage applied between the circuit points 12 and 13 and corresponds to the voltage present between the two inputs of the first differential amplifier 5. U_{ref} is the reference voltage connected to the input 15. OUT is the resulting signal that can be picked off at the output 16, and is available electrically isolated from the input signals.

Consequently, in this embodiment a magneto-sensitive electrical isolation is achieved with the release of portions of the input Sign. 1 by the input signal Sign. 2.

Figure 3 shows a third exemplary embodiment of the invention. In this exemplary embodiment, an input signal Sign. 1 is fed to the illustrated circuit via a first signal line, an input signal Sign. 2 is fed to the illustrated circuit via a second signal line, and the input signal Sign. 2 is also fed to the circuit via a third signal line. These input signals are to be combined with one another, so that by means of the signal Sign. 2, parts of the signal Sign. 1 are selected and a chipselect signal is also generated.

For this purpose the above mentioned input signals are fed to a transmitter Ü where, using respective conductor loops, they are brought into the vicinity of respective magneto-sensitive detectors 1, 2 and 3. These detectors are a component of a parallel circuit with two paths provided between a power supply voltage connection VSS and ground. Magneto-sensitive detectors 1 and 2 in the form of a series circuit are located in the first path. The second path contains magneto-sensitive detectors 3 and 4 which also form a series circuit. From the connection point 12 between the magneto-sensitive

detectors 1 and 2 a signal connection leads to an input of a first differential amplifier 5. Its other input is connected with the connection point 13 between the two magneto-sensitive detectors 3 and 4.

Connected to the output of the first differential amplifier 5 are two additional differential amplifiers 17 and 18 that are located parallel to each other. A reference voltage U_{ref1} which is derived from a reference voltage input 19 is fed to the other input of the differential amplifier 17. The other input of the differential amplifier 18 is connected with an input 20 to which a reference voltage U_{ref2} is applied.

The output of the differential amplifier 17 is connected with an input of an additional differential amplifier 21. The output of the differential amplifier 18 is fed to the other input of the differential amplifier 21.

The output signal of the differential amplifier 21 is made available in the form of an OUT resulting signal at the output 22 and corresponds to a portion of the input signal Sign. 1 selected by means of the input signal Sign. 2. The resulting signal OUT is available electrically isolated from the above mentioned input signals.

The output signal of the differential amplifier 18 is fed to an output connection 23 and corresponds to the desired chipselect signal CS. This signal is also available in an electrically isolated manner from the input signals.

In Figure 3, the signal waveforms of the signals that are presented in the block diagram are shown below the block diagram. The top two signal waveforms correspond to the input signals Sign. 1 and Sign. 2. The signal U_{out} applied between the inputs of the first differential amplifier is indicated in the middle of the illustration, as are the reference voltages U_{ref1} and U_{ref2}. The resulting signals OUT and CS made available at the outputs 22 and 23 are shown in the bottom two illustrations.

Figure 4 shows a fourth exemplary embodiment of the invention. In this exemplary embodiment, the three input signals Sign. 1, Sign. 2 and Sign. 3 fed to the illustrated signals are logically combined with one another in the sense of an electrically isolated channel switching operation, so that signals are made available on the output side which are placed either in a channel 1 or in a channel 2 or in a channel 3.

For this purpose, the above mentioned input signals are fed to a transmitter Ü where they are each conducted by means of a conductor loop to the vicinity of

respective magneto-sensitive detectors 1, 2 and 4. These detectors are a component of a parallel circuit with two paths placed between a power supply voltage connection V_{SS} and the ground. In the first path there are magneto-sensitive detectors 1 and 2 in the form of a series circuit. The second path contains magneto-sensitive detectors 3 and 4 which also form a series circuit. From the connection point 12 between the magneto-sensitive detectors 1 and 2 a signal connection leads to an input of the first differential amplifier 5. Its other input is connected to the connection point 13 between the two magneto-sensitive detectors 3 and 4.

Connected to the output of the first differential amplifier 5 are three additional differential amplifiers 24, 25 and 26 which are arranged parallel to one another. A reference voltage U_{ref1} derived from a reference voltage input 27 is fed to the other input of the differential amplifier 24. The other input of the differential amplifier 25 is connected with an input 28, to which a reference voltage U_{ref2} is applied. A reference voltage U_{ref3} derived from a reference voltage input 29 is fed to the other input of the differential amplifier 26.

A resulting signal OUT1 can be picked off at the output 30 of the differential amplifier 24, a resulting signal OUT2 can be picked off at the output of the differential amplifier 25 and a resulting signal OUT3 can be picked off at the output of the differential amplifier 26. The resulting signal OUT1 corresponds to the signals in channel 1, the resulting signal OUT2 to the signals in channel 2 and the resulting signal OUT3 to the signals in channel 3, whereby these signals are each available electrically isolated from the input signals Sign. 1, Sign. 2 and Sign. 3.

Below the block diagram illustrated in Figure 4 are the signal waveforms of the signals illustrated in the block diagram. From the top signal waveform it is apparent that for Sign. 2 = 0 and Sign. 3 = 1, the output signal OUT2 in the channel 2 at the output 31 will be available, that for Sign. 2 = 0 and Sign. 3 = 0, the output signal OUT1 in the channel 1 will be available at the output 30, and that for Sign. 2 = 1 and Sign. 3 = 0, the output signal OUT3 in channel 3 will be available at the output 32. The above mentioned output signals thereby each correspond to the electrically isolated input signals Sign. 1, which is forwarded by the selection of pre-determined values of Sign. 2 and Sign. 3 to the respective channel.

From the exemplary embodiments explained above, it is apparent that logic operations can be realized by an actuation of the respective desired signal combination and a switching of magneto-sensitive elements, for example giant magnetic resistance (GMR) bridges and a suitable evaluation circuitry, whereby the respective output signals are made available in electrically isolated form. These logic operations can always be realized easily and economically, if technologies of a similar type are already being used anyway in the existing circuit.

Claims

1. Method for the logic combination of signals with the following steps:

a) the signals to be combined with each other are fed on separate signal lines to a transmitter that has magneto-sensitive coupling elements, whereby each coupling element has a magneto-sensitive detector;

b) the signals to be combined with each other are each transmitted in an electrically isolated manner in the transmitter and are each detected by the magneto-sensitive detector of the coupling element;

c) the signals derived from the magneto-sensitive detectors of the coupling elements are fed to an evaluation unit, where they are evaluated;

d) resulting signals are made available at the output or the outputs of the evaluation unit.

2. Method as claimed in Claim 1, characterized by the fact that signals derived from the magneto-sensitive detectors of the coupling elements are fed to the inputs of a first differential amplifier and the determination of the resulting signal is made by evaluating the output signal of the first differential amplifier using at least one additional differential amplifier connected to the output of the first differential amplifier.

3. Method as claimed in Claim 2, characterized by the fact that in addition to the output signal of the first differential amplifier, a reference voltage signal is fed to the additional differential amplifier.

4. Device for the logic combination of signals, characterized by the fact that it has a transmitter (Ü) that has at least two magneto-sensitive coupling elements;
the coupling elements each have a respective conductor loop on the input side and each a respective magneto-sensitive detector (1, 2, 3, 4) on the output side,
the compound elements each have an input for a signal to be combined,
an evaluation unit (5-9; 5, 14, 15; 5, 17-21; 5, 24-29) is connected to the outputs of the magneto-sensitive detectors, and

the evaluation unit has one or more output connections (10, 11; 16; 22, 23; 30-32) at which resulting signals can be picked off.

5. Device as claimed in Claim 4, characterized by the fact that the transmitter (Ü) has, on the output side, a parallel connection of two magneto-sensitive detectors (1, 2, 3, 4) connected in series, that from the connecting point (12, 13) between the two magneto-sensitive detectors connected in series, a signal line leads to an input connection of a first differential amplifier (5), and that the output of the first differential amplifier (5) is connected with a first input of an additional differential amplifier, the second input of which is connected to a reference voltage source.

6. Device as claimed in Claim 5, characterized by the fact that connected to the output of the first differential amplifier is a parallel connection of a plurality of additional differential amplifiers (8, 9; 17, 18; 24-26), the respective second input of which is connected to a respective reference voltage source.

4 pages of drawings